Amendments to the Specification:

Please replace the Title of the application to the following amended Title:

DSP EXECUTION UNIT FOR EFFICIENT ALTERNATE MODES ~~OF OPERATION~~ FOR PROCESSING MULTIPLE DATA SIZES.

Please replace the paragraph beginning at page 1, line 4 with the following amended paragraph:

~~This invention~~ The present application relates to digital signal processors, and more particularly to digital signal processors for processing reduced data sizes. The present application is a divisional of Applicant's prior Application No. 09/541,116 (now issued U.S. Patent No. 6,725,350), and claims benefit of the earlier filing date of the parent application under 35 U.S.C. 120.

Please replace the paragraph beginning at page 2, line 17 with the following amended paragraph:

Figure 2 is a schematic of a digital signal processor for either n-bit or (n/2)-bit modes of operation according to an embodiment of the present invention.

Please replace the paragraphs beginning at page 3, line 1 with the following amended paragraphs:

Figure 4 is a schematic of a digital signal processor including a split multiplier for (n/2)-bit operation according to an embodiment of the present invention.

Figure 5 shows a schematic of a digital signal processor for either n-bit or (n/2)-bit modes of operation according to an alternate embodiment of the present invention.

Please replace the paragraph beginning at page 7, line 3 with the following amended paragraph:

The DSP 200 may process the selected 16-bit data sets 125, 130 in either 8-bit mode or 16-bit mode. The DSP 200 includes multiplexers 205, 210, 235, 240 and ALUs 225, 230 which may operate in parallel with the ~~multiplexer~~ multiplier 135 and support the (n/2)-bit, or 8-bit, operation of the DSP 200. The multiplexers 205, 210 receive the selected 16-bit data sets 125, 130 from the multiplexers 115, 120. The multiplexer 205 selects the appropriate 16-bit data from the input data 125, 130 and outputs 8-bit data 215. The multiplexer 210 also selects the appropriate 16-bit data sets from the input data 125, 130 and outputs 8-bit data 220. Of course, the original data from the

data bus may have been 8-bit, in which case the 8-bit data is passed through the multiplexers 115, 120, 205, 210 to the ALUs 225, 230.

Please replace the paragraph beginning at page 12, line 3 with the following amended paragraph:

Figure 5 shows a schematic of a digital signal processor for either n-bit or (n/2)-bit modes of operation according to an alternate embodiment of the present invention. The DSP 500 in Figure 5 is a modified version of the DSP 200 of Figure 2. In Figure 5, a multiplexer 505 is placed between the multiplexer 235 and the flop 140. A second multiplexer 510 is placed between the multiplexer 240 and the flop 145. The multiplexers 505 and 510 allow selection of the input to provide to the flops 140, 145. The DSP 300 of Figure 3 can be similarly modified.